ANALOG DEVICES

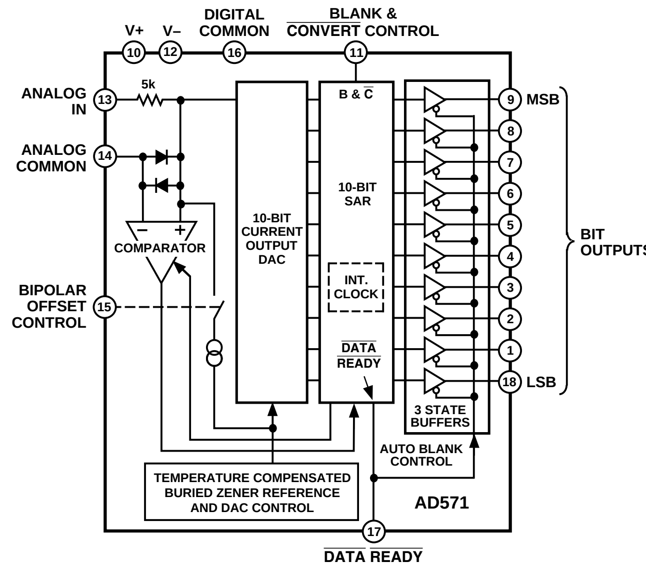
10-Bit A/D Converter

AD571*

FEATURES

Complete A/D Converter with Reference and Clock
Fast Successive Approximation Conversion: 40 µs max
No Missing Codes Over Temperature
0°C to +70°C: AD571K
–55°C to +125°C: AD571S
Digital Multiplexing: Three-State Outputs
18-Pin Ceramic DIP
Low Cost Monolithic Construction

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD571 is an 10-bit successive approximation A/D converter consisting of a DAC, voltage reference, clock, comparator, successive approximation register and output buffers—all fabricated on a single chip. No external components are required to perform a full accuracy 10-bit conversion in 40 µs.

Operating on supplies of +5 V to +15 V and –15 V, the AD571 will accepts analog inputs of 0 V to +10 V unipolar of ±5 V bipolar, externally selectable. When the BLANK and CONVERT input is driven low, the three-state outputs will be open and a conversion will commence. Upon completion of the conversion, the DATA READY line goes low and the data appears at the output. Pulling the BLANK and CONVERT input high blanks the outputs and readies the device for the next conversion. The AD571 executes a true 10-bit conversion with no missing codes in 40 µs maximum.

The AD571 is available in two version for the 0°C to +70°C temperature range, the AD571J and K. The AD571S guarantees 10-bit accuracy and no missing codes from –55°C to +125°C.

***Covered by Patent Nos. 3,940,760; 4,213,806; 4,136,349.**

PRODUCT HIGHLIGHTS

1. The AD571 is a complete 10-bit A/D converter. No external components are required to perform a conversion. Full-scale calibration accuracy of ±0.3% is achieved without external trims.
2. The AD571 is a single chip device employing the most advanced IC processing techniques. Thus, the user has at his disposal a truly precision component with the reliability and low cost inherent in monolithic construction,
3. The AD571 accepts either unipolar (0 V to +10 V) or bipolar (–5 V to +5 V) analog inputs by grounding or opening a single pin.
4. The device offers true 10-bit accuracy and exhibits no missing codes over its entire operating temperature range.
5. Operation is guaranteed with –15 V and +5 V or +15 V supplies. The device will also operate with a –12 V supply.

REV. A

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AD571—SPECIFICATIONS (T_A = +25°C, V+ = +5 V, V– = –12 V or –15 V, all voltages measured with respect to digital common, unless otherwise noted)

Model	AD571J Min	AD571J Typ	AD571J Max	AD571K Min	AD571K Typ	AD571K Max	AD571S Min	AD571S Typ	AD571S Max	Units
RESOLUTION			10			10			10	Bits
RELATIVE ACCURACY, T_A			**±1**			**±1/2**			**±1**	LSB
T_{MIN} to T_{MAX}			**±1**			**±1/2**			**±1**	LSB
FULL-SCALE CALIBRATION		±2			±2			±2		LSB
UNIPOLAR OFFSET			**±1**			**±1/2**			**±1**	LSB
BIPOLAR OFFSET			**±1**			**±1/2**			**±1**	LSB
DIFFERENTIAL NONLINEAIRTY, T_A	**10**			**10**			**10**			Bits
T_{MIN} to T_{MAX}	**9**			**10**			**10**			Bits
TEMPERATURE RANGE	0		+70	0		+70	–55		+125	°C
TEMPERATURE COEFFICIENTS										
Unipolar Offset			**±2**			**±1**			**±2**	LSB
Bipolar Offset			**±2**			**±1**			**±2**	LSB
Full-Scale Calibration[2]			**±4**			**±2**			**±5**	LSB
POWER SUPPLY REJECTION										
CMOS Positive Supply										
+13.5 V ≤ V + ≤ +16.5 V	–	–	–			**±1**	–	–	–	LSB
TTL Positive Supply										
+4.5 V ≤ V + ≤ +5.5 V			**±2**			**±1**			**±2**	LSB
Negative Supply										
–16.0 V ≤ V – ≤ –13.5 V			**±2**			**±1**			**±2**	LSB
ANALOG INPUT IMPEDANCE	**3.0**	5.0	**7.0**	**3.0**	5.0	**7.0**	**3.0**	5.0	**7.0**	kΩ
ANALOG INPUT RANGES										
Unipolar	0		+10	0		+10	0		+10	V
Bipolar	–5		+5	–5		+5	–5		+5	V
OUTPUT CODING										
Unipolar	Positive True Binary			Positive True Binary			Positive True Binary			
Bipolar	Positive True Offset Binary			Positive True Offset Binary			Positive True Offset Binary			
LOGIC OUTPUT										
Output Sink Current										
(V_{OUT} = 0.4 V max, T_{MIN} to T_{MAX})	**3.2**			**3.2**			**3.2**			mA
Output Source Current[1]										
(V_{OUT} = 2.4 V max, T_{MIN} to T_{MAX})	**0.5**			**0.5**			**0.5**			mA
Output Leakage			**±40**			**±40**			**±40**	µA
LOGIC INPUT										
Input Current			**±100**			**±100**			**±100**	µA
Logic "1"	**2.0**			**2.0**			**2.0**			V
Logic "0"			**0.8**			**0.8**			**0.8**	V
CONVERSION TIME, T_{MIN} to T_{MAX}	**15**	25	**40**	**15**	25	**40**	**15**	25	**40**	µs
POWER SUPPLY										
V+	**+4.5**	+5.0	**+7.0**	**+4.5**	**+5.0**	**+16.5**	**+4.5**	+5.0	**+7.0**	V
V–	**–12.0**	–15	**–16.5**	**–12.0**	–15	**–16.5**	**–12.0**	–15	**–16.5**	V
OPERATING CURRENT										
V+		7	**10**		7	**10**		7	**10**	mA
V–		9	**15**		9	**15**		9	**15**	mA
PACKAGE OPTION[2]										
Ceramic DIP (D-18)		AD571JD			AD571KD			AD571SD		

NOTES

[1]The data output lines have active pull-ups to source 0.5 mA. The $\overline{\text{DATA READY}}$ line is open collector with a nominal 6 kΩ internal pull-up resistor.

[2]For details on grade and package offerings for SD-grade in accordance with MIL-STD-883, refer to Analog Devices' Military Products databook or current /883B data sheet.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

V+ to Digital Common
AD571J . . . . 0 V to +7 V
AD571K . . . . 0 V to +16.5 V
V– to Digital Common . . . . 0 V to –16.0 V
Analog Common to Digital Common . . . . ±1 V
Analog Input to Analog Common . . . . ±15 V
Control Inputs . . . . 0 V to V+
Digital Outputs (Blank Mode) . . . . 0 V to V+
Power Dissipation. . . . . 800 mW

CIRCUIT DESCRIPTION

The AD571 is a complete 10-bit A/D converter which requires no external components to provide the complete successive-approximation analog-to-digital conversion function. A block diagram of the AD571 is shown on front page of this data sheet. Upon receipt of the $\overline{\text{CONVERT}}$ command, the internal 10-bit current output DAC is sequenced by the I^2L successive-approximation register (SAR) from its most-significant bit (MSB) to least-significant bit (LSB) to provide an output current which accurately balances the input signal current through the 5 kΩ input resistor. The comparator determines whether the addition of each successively-weighted bit current causes the DAC current sum to be greater or less than the input current; if the sum is less the bit is left on, if more, the bit is turned off. After testing all the bits, the SAR contains a 10-bit binary code which accurately represents the input signal to within ±1/2 LSB (0.05%).

Upon completion of the sequence, the SAR sends out a $\overline{\text{DATA READY}}$ signal (active low), which also brings the three-state buffers out of their "open" state, making the bit output lines become active high or low, depending on the code in the SAR. When the BLANK and $\overline{\text{CONVERT}}$ line is brought high, the output buffers again go "open", and the SAR is prepared for another conversion cycle. Details of the timing are given in the Control and Timing section.

The temperature compensated buried Zener reference provides the primary voltage reference to the DAC and guarantees excellent stability with both time and temperature. The bipolar offset input controls a switch which allows the positive bipolar offset current (exactly equal to the value of the MSB less 1/2 LSB) to be injected into the summing (+) node of the comparator to offset the DAC output. Thus the nominal 0 V to +10 V unipolar input range becomes a –5 V to +5 V range. The 5 kΩ thin-film input resistor is trimmed so that with a full-scale input signal, an input current will be generated which exactly matches the DAC output with all bits on. (The input resistor is trimmed slightly low to facilitate user trimming, as discussed on the next page.)

POWER SUPPLY SELECTION

The AD571 is designed for optimum performance using a +5 V and –15 V supply, for which the AD571J and AD571S are specified. AD571K will also operate with up to a +15 V supply, which allows direct interface to CMOS logic. The input logic threshold is a function of V+ as shown in Figure 1. The supply current drawn by the device is a function of both V+ and the operating mode (BLANK or CONVERT). These supply currents variations are shown in Figure 2. The supply currents change only moderately over temperature as shown in Figure 6.

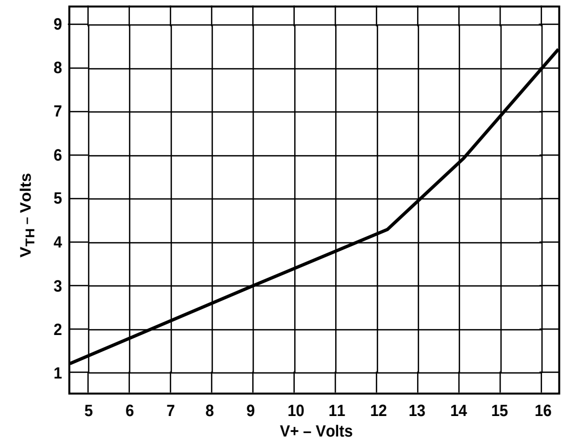


Figure 1. Logic Threshold (AD571K Only)

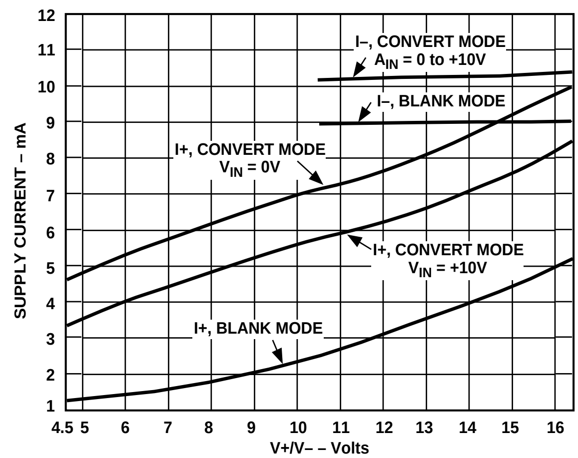


Figure 2. Supply Currents vs. Supply Levels and Operating Modes

CONNECTING THE AD571 FOR STANDARD OPERATION

The AD571 contains all the active components required to perform a complete A/D conversion. For most situations, all that is necessary is connection of the power supply (+5 V and –15 V), the analog input, and the conversion start pulse. However, there are some features and special connections which should be considered for optimum performance. The functional pinout is shown in Figure 3.

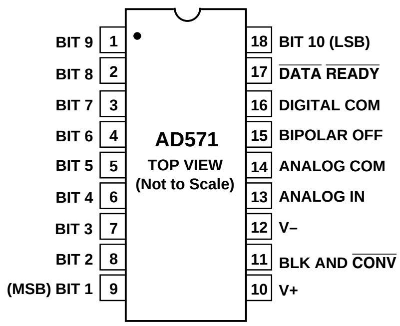


Figure 3. AD571 Pin Connections

FULL-SCALE CALIBRATION

The 5 kΩ thin-film input resistor is laser trimmed to produce a current which matches the full-scale current of the internal DAC—plus about 0.3%—when a full-scale analog input voltage of 9.990 volts (10 volts—1 LSB) is applied at the input. The input resistor is trimmed in this way so that if a fine trimming potentiometer is inserted in series with the input signal, the input current at the full-scale input voltage can be trimmed down to match the DAC full-scale current as precisely as desired. However, for many applications the nominal 9.99 volt full scale can be achieved to sufficient accuracy by simply inserting a 15 Ω resistor in series with the analog input to Pin 13. Typical full-scale calibration error will then be about ±2 LSB or ±0.2%. If a more precise calibration is desired, a 50 Ω trimmer should be used instead. Set the analog input at 9.990 volts, and set the trimmer so that the output code is just at the transition between 1111111110 and 1111111111. Each LSB will then have a weight of 9.766 mV. If a nominal full scale of 10.24 volts is desired (which makes the LSB have a value of exactly 10.00 mV), a 100 Ω resistor in series with a 100 Ω trimmer (or a 200 Ω trimmer with good resolution) should be used. Of course, larger full-scale ranges can be arranged by using a larger input resistor, but linearity and full-scale temperature coefficient may be compromised if the external resistor becomes a sizable percentage of 5 kΩ.

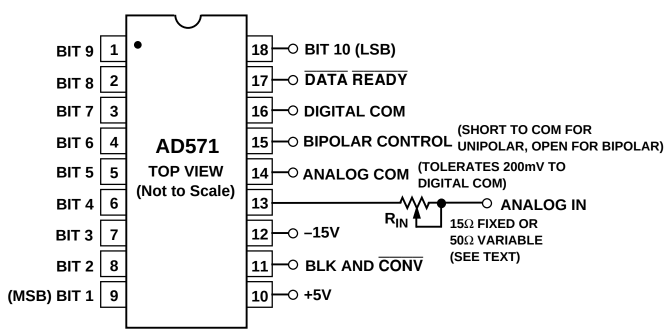


Figure 4. Standard AD571 Connections

BIPOLAR OPERATION

The standard unipolar 0 V to +10 V range is obtained by shorting the bipolar offset control pin to digital common. If the pin is left open, the bipolar offset current will be switched into the comparator summing node, giving a –5 V to +5 V range with an offset binary output code. (–5.00 volts in will give a 10-bit code of 0000000000; an input of 0.00 volts results in an output code of 1000000000 and 4.99 volts at the input yields the 1111111111). The bipolar offset control input is not directly TTL compatible, but a TTL interface for logic control can be constructed as shown in Figure 5.

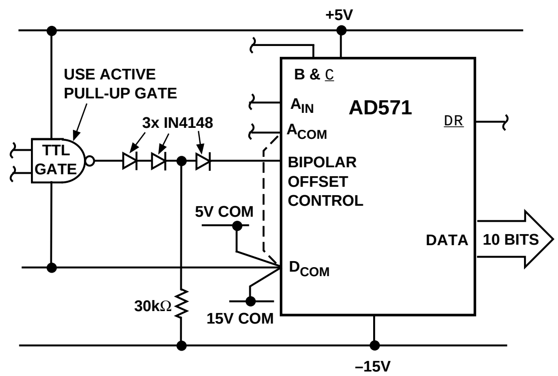


Figure 5. Bipolar Offset Controlled by Logic Gate
Gate Output = 1: Unipolar 0 V–10 V Input Range
Gate Output = 0: Bipolar ±5 V Input Range

COMMON-MODE RANGE

The AD571 provides separate analog and digital common connections. The circuit will operate properly with as much as ±200 mV of common-mode range between the two commons. This permits more flexible control of system common bussing and digital and analog returns.

In normal operation the analog common terminal may generate transient currents of up to 2 mA during a conversion. In addition, a static current of about 2 mA will flow into analog common in the unipolar mode after a conversion is complete. An additional 1 mA will flow in during a blank interval with zero analog input. The analog common current will be modulated by the variations in input signal.

The absolute maximum voltage rating between the two commons is ±1 volt. We recommend that a parallel pair of back-to-back protection diodes can be connected between the commons if they are not connected locally.

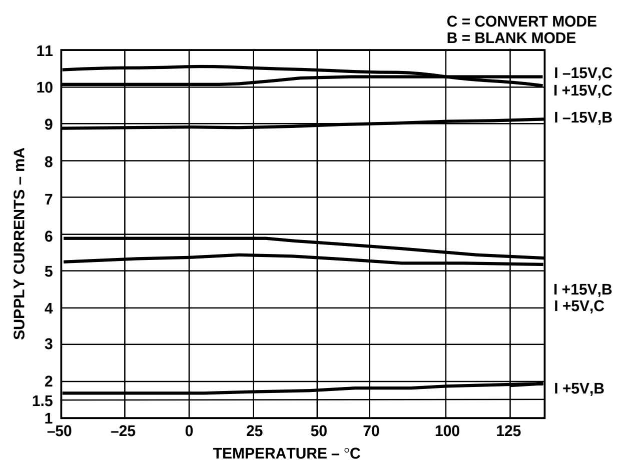


Figure 6. AD571 Power Supply Current vs. Temperature

ZERO OFFSET

The apparent zero point of the AD571 can be adjusted by inserting an offset voltage between the analog common of the device and the actual signal return or signal common. Figure 7 illustrates two methods of providing this offset. Figure 7a shows how the converter zero may be offset by up to ±3 bits to correct the device initial offset and/or input signal offsets. As shown, the circuit gives approximately symmetrical adjustment in unipolar mode. In bipolar mode R2 should be omitted to obtain a symmetrical range.

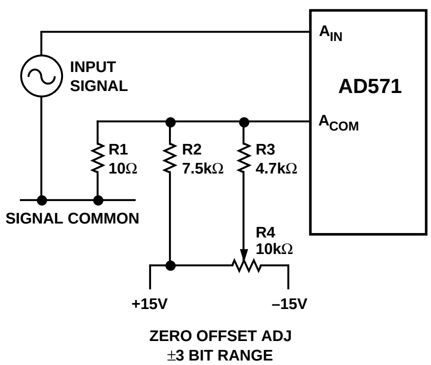


Figure 7a.

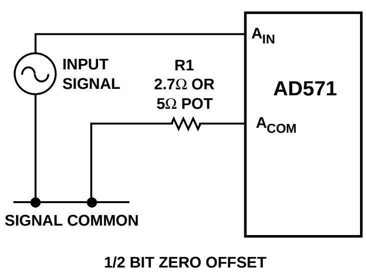


Figure 7b.

Figure 8 shows the nominal transfer curve near zero for an AD571 in unipolar mode. The code transitions are at the edges of the nominal bit weights. In some applications it will be preferable to offset the code transitions so that they fall between the nominal bit weights, as shown in the offset characteristics. This offset can easily be accomplished as shown in Figure 7b. At balance (after a conversion) approximately 2 mA flows into the analog common terminal. A 2.7 Ω resistor in series with this terminal will result in approximately the desired 1/2 bit offset of the transfer characteristics. The nominal 2 mA analog common current is not closely controlled in production. If high accuracy is required, a 5 Ω potentiometer (connected as a rheostat) can be used as R1. Additional negative offset range may be obtained by using larger values of R1. Of course, if the zero transition point is changed, the full-scale transition point will also move. Thus, if an offset of 1/2 LSB is introduced, full-scale trimming as described on previous page should be done with an analog input of 9.985 volts.

NOTE: During a conversion transient currents from the analog common terminal will disturb the offset voltage. Capacitive decoupling should not be used around the offset network. These transients will settle as appropriate during a conversion. Capacitive decoupling will "pump up" and fail to settle resulting in conversion errors. Power supply decoupling which returns to analog signal common should go to the signal input side of the resistive offset network.

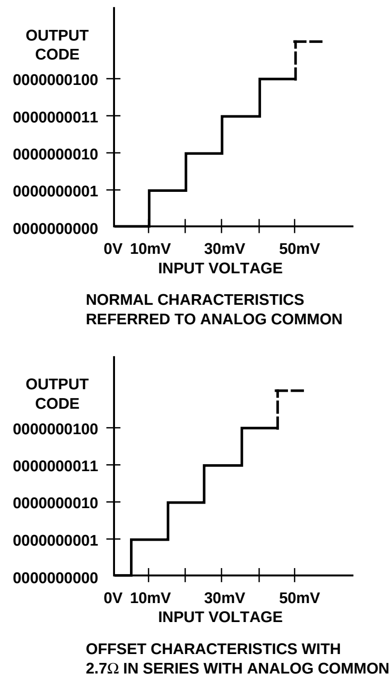


Figure 8. AD571 Transfer Curve—Unipolar Operation (Approximate Bit Weights Shown for Illustration, Nominal Bit Weights ~ 9.766 mV)

BIPOLAR CONNECTION

To obtain the bipolar –5 V to +5 V range with an offset binary output code the bipolar offset control pin is left open.

A –5.0 volt signal will give a 10-bit code of 0000000000; an input of 0.00 volts results in an output code of 1000000000; +4.99 volts at the input yields 1111111111. The nominal transfer curve is shown in Figure 9.

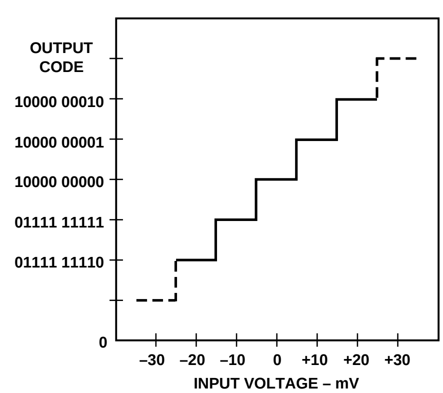


Figure 9. AD571 Transfer Curve—Bipolar Operation

CONTROL AND TIMING OF THE AD571

There are several important timing and control features on the AD571 which must be understood precisely to allow optimal interfacing to microprocessor or other types of control systems. All of these features are shown in the timing diagram in Figure 10.

The normal standby situation is shown at the left end of the drawing. The BLANK and $\overline{\text{CONVERT}}$ (B & $\overline{\text{C}}$) line is held high, the output lines will be "open", and the $\overline{\text{DATA READY}}$ ($\overline{\text{DR}}$) line will be high. This mode is the lowest power state of the device (typically 150 mW). When the (B & $\overline{\text{C}}$) line is brought low, the conversion cycle is initiated; but the $\overline{\text{DR}}$ and data lines do not change state. When the conversion cycle is complete, the $\overline{\text{DR}}$ line goes low, and within 500 ns, the data lines become active with the new data.

About 1.5 µs after the B & $\overline{\text{C}}$ line is again brought high, the $\overline{\text{DR}}$ line will go high and the data lines will go open. When the B & $\overline{\text{C}}$ line is again brought low, a new conversion will begin. The minimum pulse width for the B & $\overline{\text{C}}$ line to blank previous data and start a new conversion is 2 µs. If the B & $\overline{\text{C}}$ line is brought high during a conversion, the conversion will stop, and the $\overline{\text{DR}}$ and data lines will not change. If a 2 µs or longer pulse is applied to the B & $\overline{\text{C}}$ line during a conversion, the converter will clear and start a new conversion cycle.

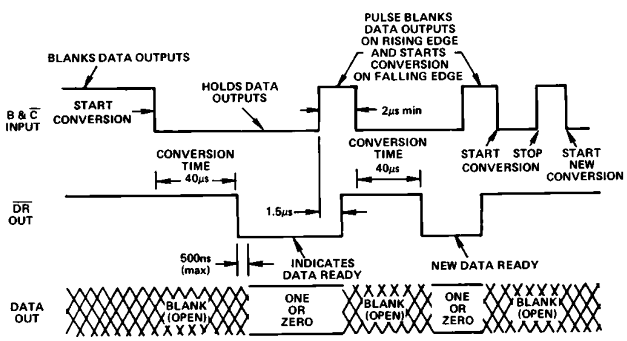


Figure 10. AD571 Timing and Control Sequences

CONTROL MODES WITH BLANK AND $\overline{\text{CONVERT}}$

The timing sequence of the AD571 discussed above allows the device to be easily operated in a variety of systems with differing control modes. The two most common control modes, the Convert Pulse Mode and the Multiplex Mode, are illustrated here.

Convert Pulse Mode–In this mode, data is present at the output of the converter at all times except when conversion is taking place. Figure 11 illustrates the timing of this mode. The BLANK and $\overline{\text{CONVERT}}$ line is normally low and conversions are triggered by a positive pulse. A typical application for this timing mode is shown in Figure 14, in which µP bus interfacing is easily accomplished with three-state buffers.

Multiplex Mode—In this mode the outputs are blanked except when the device is selected for conversion and readout; this timing is shown in Figure 12. A typical AD571 multiplexing application is shown in Figure 15.

This operating mode allows multiple AD571 devices to drive common data lines. All BLANK and $\overline{\text{CONVERT}}$ lines are held high to keep the outputs blanked. A single AD571 is selected, its BLANK and $\overline{\text{CONVERT}}$ line is driven low and at the end of conversion, which is indicated by $\overline{\text{DATA READY}}$ going low, the conversion result will be present at the outputs. When this data has been read from the 10-bit bus, BLANK and $\overline{\text{CONVERT}}$ is restored to the blank mode to clear the data bus for other converters. When several AD571s are multiplexed in sequence, a new conversion may be started in one AD571 while data is being read from another. As long as the data is read and the first AD571 is cleared within 15 µs after the start of conversion of the second AD571, no data overlap will occur.

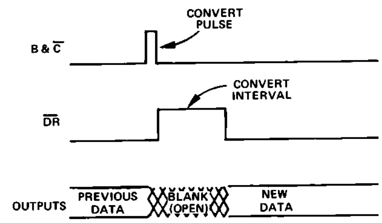


Figure 11. Convert Pulse Mode

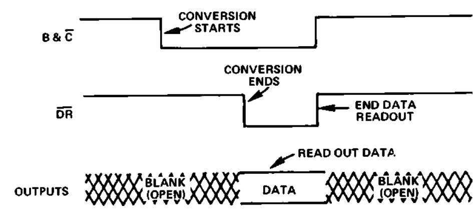


Figure 12. Multiplex Mode

SAMPLE-HOLD AMPLIFIER CONNECTION TO THE AD571

Many situations in high-speed acquisition systems or digitizing of rapidly changing signals require a sample-hold amplifier (SHA) in front of the A-D converter. The SHA can acquire and hold a signal faster than the converter can perform a conversion. A SHA can also be used to accurately define the exact point in time at which the signal is sampled. For the AD571, a SHA can also serve as a high input impedance buffer.

Figure 13 shows the AD571 connected to the AD582 monolithic SHA for high speed signal acquisition. In this configuration, the AD582 will acquire a 10 volt signal in less than 10 µs with a droop rate less than 100 µV/ms. The control signals are arranged so that when the control line goes low, the AD582 is put into the "hold" mode, and the AD571 will begin its conversion cycle. (The AD582 settles to final value well in advance of the first comparator decision inside the AD571). The $\overline{\text{DATA READY}}$ line is fed back to the other side of the differential input control gate so that the AD582 cannot come out of the "hold" mode during the conversion cycle. At the end of the conversion cycle, the $\overline{\text{DATA READY}}$ line goes low, automatically placing the AD582 back into the sample mode. This feature allows simple control of both the SHA and the A-D converter with a single line. Observe carefully the ground, supply, and bypass capacitor connections between the two devices. This will minimizes ground noise and interference during the conversion cycle to give the most accurate measurements.

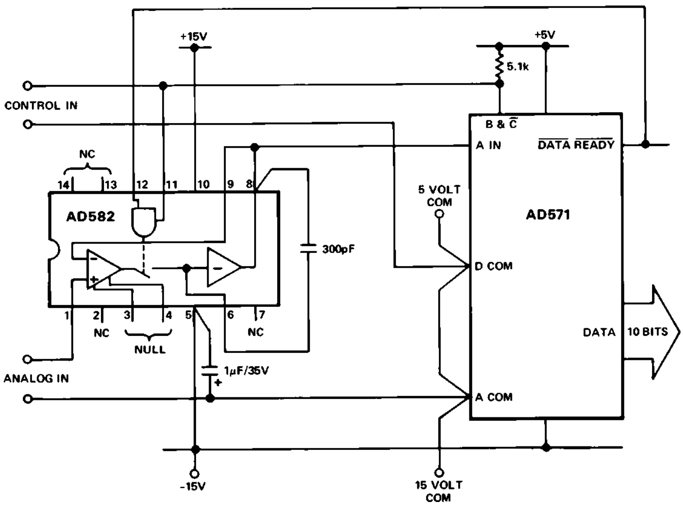


Figure 13. Sample-Hold Interface to the AD571

INTERFACING THE AD571 TO A MICROPROCESSOR

The AD571 can easily be arranged to be driven from standard microprocessor control lines and to present data to any standard microprocessor bus (4-, 8-, 12- or 16-bit) with a minimum of additional control components. The configuration shown in Figure 14 is designed to operate with an 8-bit bus and standard 8080 control signals.

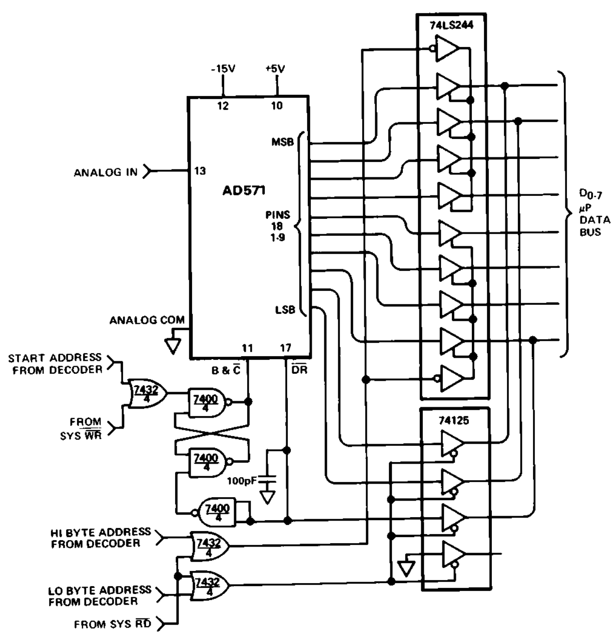


Figure 14. Interfacing AD571 to an 8-Bit Bus (8080 Control Structure)

The input control circuitry shown is required to ensure that the AD571 receives a sufficiently long B & $\overline{C}$ input pulse. When the converter is ready to start a new conversion, the B & $\overline{C}$ line is low, and $\overline{DR}$ is low. To command a conversion, the start address decode line goes low, followed by $\overline{WR}$. The B & $\overline{C}$ line will now go high, followed about 1.5 μs later by $\overline{DR}$. This resets the external flip-flop and brings B & $\overline{C}$ back to low, which initiates the conversion cycle. At the end of the conversion cycle, the $\overline{DR}$ line goes low, the data outputs will become active with the new data and the control lines will return to the standby state. The 100 pF capacitor slows down the $\overline{DR}$ line enough to be used as a latch signal for data outputs. The new data will remain active until a new conversion is commanded. The self-pulsing nature of this circuit guarantees a sufficient convert pulse width.

This new data can now be presented to the data bus by enabling the three-state buffers when desired. A data word (8-bit or 2-bit) is loaded onto the bus when its decoded address goes low and the $\overline{RD}$ line goes low. This arrangement presents data to the bus "left-justified," with the highest bits in the 8-bit word; a "right-justified" data arrangement can be set up by a simple re-wiring. Polling the converter to determine if conversion is complete can be done by addressing the gate which buffers the $\overline{DR}$ line, as shown. In this configuration, there is no need for additional buffer register storage: the data can be held indefinitely in the AD571, since the B & $\overline{C}$ line is continually held low.

BUS INTERFACING WITH A PERIPHERAL INTERFACE CIRCUIT

An improved technique for interfacing to a μP bus involves the use of special peripheral interfacing circuits (or I/O devices), such as the MC6821 Peripheral Interface Adapter (PIA). Shown in Figure 15 is a straightforward application of a PIA to multiplex up to 8 AD571 circuits. The AD571 has 3-state outputs,

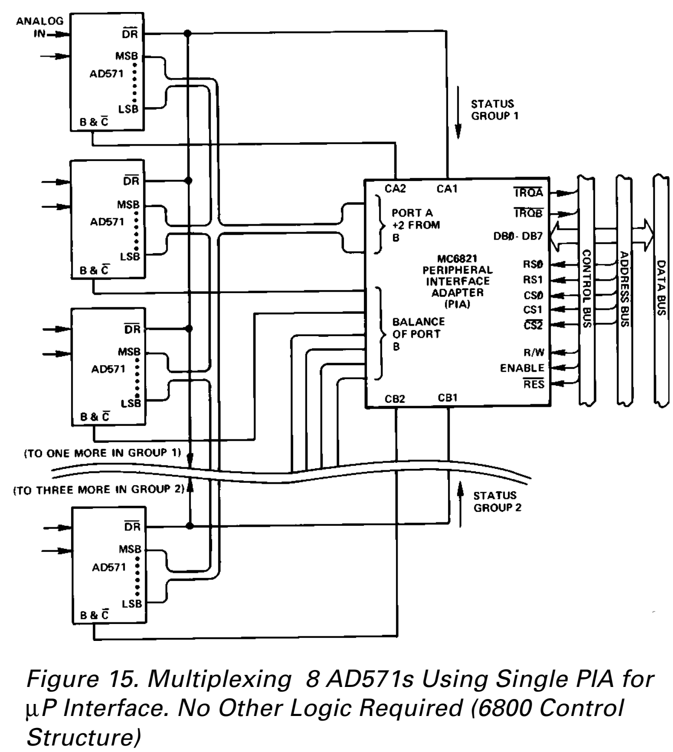


Figure 15. Multiplexing 8 AD571s Using Single PIA for μP Interface. No Other Logic Required (6800 Control Structure)

hence the data bit outputs can be paralleled, provided that only one converter at a time is permitted to be the active state. The $\overline{DATA}$ $\overline{READY}$ output of the AD571 is an open collector with resistor pull-up, thus several $\overline{DR}$ lines can be wire-ored to allow indication of the status of the selected device. One of the 8-bit ports of the PIA is combined with 2 bits from the other port and programmed as a 10-bit input port. The remaining 6 bits of the second port are programmed as outputs and along

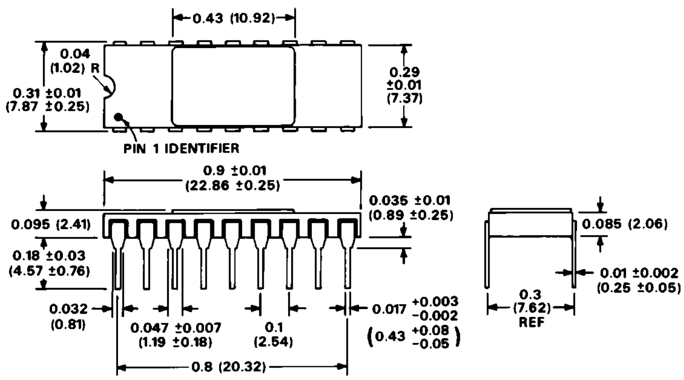
with the 2 control bits (which act as outputs), are used to control the 8 AD571s. When a control line is in the "1" or high state, the ADC will be automatically blanked. That is, its outputs will be in the inactive open state. If a single control line is switched low, its ADC will convert and the outputs will automatically go active when the conversion is complete. The result can then be read from the two peripheral ports; when the next conversion is desired, a different control line can be switched to zero, blanking the previously active port at the same time. Subsequently, this second device can be read by the microprocessor, and so-forth. The status lines are wire-ored in 2 groups and connected to the two remaining control pins. This allows a conversion status check to be made after a convert command, if necessary. The ADCs are divided into two groups to minimize the loading effect of the internal pull-up resistors on the $\overline{\text{DATA READY}}$ buffers.

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OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

18-Lead Ceramic Dual-In-Line Package



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